

In the claims:

Kindly rewrite the claims to read as follows:

1. (Currently amended) A method for forming reception pulses in a receiver operating according to the IrDA standard wherein ~~the~~ output signals of an upstream comparator that recognizes light pulses are newly formed and output as pulses for evaluation by means of a downstream arrangement, ~~characterized in that wherein:~~ in a first step ~~the~~, an input signal delivered by an upstream comparator is delayed, ~~in that;~~ generation of a time reference controlled by the input signal is started, ~~in that;~~ controlled by the input signal delayed in the first step, ~~the~~ forming of an output pulse is started, ~~in that on;~~ upon completion of the generation of the time reference, ~~an examination of a level of the input signal level is examined-conducted~~ which carries out a back-reference to duration of the received-output pulse duration; and ~~in that~~ subject to ~~the~~ results of the examination, the duration of the output pulse is adjusted.
2. (Currently amended) The method according to claim 1, wherein the delay of the input signal delivered by the upstream comparator is done in a first and a second partial step and that between the ~~delay~~ first and second partial steps, a regeneration of the signal is carried out.
3. (Currently amended) The method according to claim 1, wherein the generation of the time reference is started by the input signal or the input signal delayed in ~~the~~ a first partial step.
4. (Currently amended) The method according to claim 1, wherein the forming of the output ~~signal-pulse~~ is done such that ~~the~~ forming of a first pulse and a second pulse is started in parallel and subject to the examination of the input signal level either the first or the second pulse is emitted at the output.
5. (Currently amended) An arrangement for forming reception signals in a receiver operating according to the IrDA standard wherein the output signals of an upstream comparator that recognizes light pulses are newly formed for evaluation by a downstream arrangement, wherein ~~the~~ an input (18) of a delay arrangement (4) is connected to ~~the~~ an input of the arrangement for forming reception pulses INP (2), for supply of ~~the~~ a comparator signal, wherein a first output (19) of the delay arrangement (4) is connected to a first input (21) of a down stream

output pulse producing arrangement (6) and ~~the~~ a second output of the delay arrangement (20) is connected to a time reference generating arrangement (5), wherein ~~the~~ an output of the time reference generating arrangement (5) is connected to a second input (22) of the output pulse producing arrangement (6) and, wherein ~~the~~ an output (23) of the output pulse producing arrangement (6) is connected to the output OUT (3) of the arrangement for forming reception pulses (1).

6. (Currently amended) The arrangement according to claim 5, wherein the delay arrangement (4) is comprised of a series connection of a first and a second delay arrangement ~~part (10 and 11) parts~~ parts and an arrangement for pulse reconstruction (12) installed between the ~~two~~ first and second delay arrangements (10 and 11) parts.

7. (Currently amended) The arrangement according to Claim 5, wherein the output pulse producing arrangement (6) is comprised of a circuit for forming a first pulse (14), a circuit for forming a second impulse (15), a circuit for examining the input signal level (13) and a selection circuit (16).

8. (Currently amended) The arrangement according to claim 6 wherein ~~a~~ the delay arrangement (10 ~~or 11~~) ~~comprised of~~ comprises a p-channel transistor whose gate contact is connected to an input of a logical NAND circuit and via a negator to ~~the~~ an input "Input" whose source contact is connected to ~~the~~ a potential VDDa and whose drain contact is connected to ~~the~~ an input IBIA of the delay arrangement and to the input of a Schmitt trigger, a Schmitt trigger (24) whose negated output is connected to ~~the~~ a second output of the logical NAND circuit and the logical NAND circuit whose negative output is connected to ~~the~~ an output of the delay arrangement "Output".

9. (Currently amended) The arrangement according to claim 6, wherein in an arrangement for pulse construction (12) and for forming a first pulse (14), a second pulse (15) and the time reference generation, (5) a respective input "Input" is connected to a negator, wherein ~~the~~ an output of the negator is connected to ~~the~~ a first input of a downstream first NAND circuit and a series connection comprised of three negators whose output is connected to ~~the~~ a second input of the first NAND circuit, wherein ~~the~~ an output of the first NAND circuit is connected to a first input of a second NAND circuit, wherein ~~the~~ an input IBIA of the arrangement is connected to ~~the~~ a drain contact of a p-channel transistor and is connected via a Schmitt-trigger to ~~the~~ a first

input of a NOR circuit, wherein ~~the~~an input POC of the arrangement is connected to ~~the~~a second input of the NOR circuit, wherein ~~the~~an output of the NOR circuit is connected to ~~the~~a first input of ~~the~~a third NAND circuit, wherein ~~the~~an output of the third NAND circuit is connected to the second input of the second NAND circuit, via a negator to ~~the~~a gate contact of the p-channel transistor whose source contact is connected to ~~the~~a potential VDDa, and to ~~the~~an output "Output" of the arrangement and wherein ~~the~~an output of the second NAND-circuit is connected to ~~the~~a second input of the third NAND circuit.